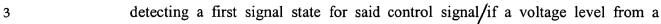
We claim:

- 1 1. A method for transmitting a control signal on a bus, said control signal having
- 2 two signal states, said method comprising the steps of:

transferring a first signal state for said control signal by adjusting a voltage level from a previous time interval; and

- transferring a second signal state by maintaining said voltage level from the
- 6 previous time interval.
- 1 2. The method of claim 1, further comprising the step of maintaining said voltage 2 level from the previous time interval using a memory element.
 - 3. The method of claim 1, further comprising the step of ensuring that only a single node connected to said bus can assert said control signal in a given time interval.
 - 4. The method of claim 1, wherein said bus is on a system-on-chip (SoC).
 - 5. The method of claim 1, wherein said bus is on a printed circuit board (PCB).
- 1 6. The method of claim 1, wherein said adjusting step further comprises the step of
- 2 transitioning from a first voltage level to a second voltage level.
- 1 7. The method of claim/1, wherein said adjusting step further comprises the step of
- 2 applying a high logic level to an exclusive-OR gate with said voltage level from the previous
- 3 time interval to determine the signal level to be asserted in the current time interval.
- 1 8. A method for receiving a control signal on a bus, said control signal having two
- 2 signal states, said method comprising the steps of:





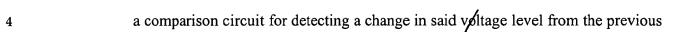
- previous time interval is adjusted; and 4
- detecting a second signal state if said voltage level from the previous time interval 5
- 6 is maintained.

The method of claim 8, further comprising the step of maintaining said control signal value at said voltage level from said previous time interval when no node drives said bus.

- 10. The method of claim 9, further comprising the step of compensating for leakage 1
- and cross-coupling effects. 2
- _1 The method of claim 8, further comprising the step of maintaining said voltage 11. level from the previous time interval using a memory element.
 - The method of claim 8, wherein said bus is on a system-on-chip (SoC). 12.
 - 13. The method of claim 8, wherein said bus is on a printed circuit board (PCB).
 - The method of claim 8, wherein said adjusted voltage level is a transitioning from 14. a first voltage level to a second voltage level.
 - The method of claim 8/ wherein said first detecting step further comprises the step 15. 1
 - of applying said received control signal state to an exclusive-OR gate with said voltage level 2
 - 3 from the previous time interval to/determine the signal level to be asserted in the current time
 - interval. 4

- 16. A device for communicating a control signal on a bus, said control signal having 1
- two signal states, said device comprising: . 2
 - a memory element for maintaining a voltage level from a previous time interval: 3





- 5 time interval indicating an assertion of said control signal by another device; and
- an adjustment circuit for changing said voltage level from the previous time
- 7 interval indicating an assertion of said control signal by another device.

Y .

- 17. The device of claim 16, wherein said memory element is a latch.
- 1 18. The device of claim 16, further comprising a circuit that ensures that only a single device connected to said bus can assert said control/signal in a given time interval.
- 1 19. The device of claim 16, wherein said bus is on a system-on-chip (SoC).
 - 20. The device of claim 16, wherein said bus is on a printed circuit board (PCB).
 - 21. The device of claim 16, wherein said change in said voltage level from the previous time interval is a change from a first voltage level to a second voltage level.
 - 22. The device of claim 16, wherein said adjustment circuit is an exclusive-OR gate.
 - 23. The device of claim 16, wherein said comparison circuit is an exclusive-OR gate.